REMARKS

Claims 131-146 are pending. Claims 131-146 were rejected under the judicially created doctrine of double patenting as being unpatentable over U.S. Patent No. 5,560,028. Thus, in response, Applicants submit the attached terminal disclaimer. It is submitted that the applicants have the right to seen broader claim coverage and/or claim coverage for different aspects of the invention.

Claims 131-138 and 145 were rejected under 35 U.S. C. 112, ¶1 for failing to disclose "mapping 'instructions slots' to the execution units" in the specification. Applicants respectfully traverse this rejection.

I. The Specification

The specification clearly discloses mapping instructions to pipeline execution units. First, in Fig. 3 an embodiment of the invention illustrates a 512 bit wide register 130 representing a line of memory cell in a cache. P. 9, lines 8-10. As shown, the register 130 includes instruction words W0 to W7, at the specific locations shown. P. 9, lines 12-13.

Second, the specification discloses in an embodiment, that groups of instruction words are dispatched to pipelines. Specifically, the specification discloses that instructions words W0 to W7 within register 130 are sorted into groups as described in the related application. P. 9, lines 13-16. The instruction words in a group of instructions are then dispatched in parallel. P. 9, lines 16-23. In Fig. 3, instruction words W0, W1, and W2 are illustrated forming Group 1, instruction words W3, W4, and W5 are illustrated forming Group 2, and instruction words W6 and W7 are illustrated forming Group 3. The related application illustrates that grouping can be performed with an "S-bit." U.S. Pat. No. 5,560,028, Fig. 10.

Third, the specification discloses mapping of instruction words to pipeline execution units. As shown in an example in Fig. 3, Group 2 instruction words W3, W4, and W5 are mapped to pipeline execution units 201, 203, and 206, respectively. The pipelines these instructions are mapped to are specified in this embodiment as "pipeline numbers" 1, 3, and 6, respectively. As also shown in Fig. 3, Group 3 instruction words W6 and W7 have "pipeline numbers" 1 and 6 respectively. Accordingly, instruction word W6 will be sent to pipeline execution unit 201 and W7 will be sent to pipeline execution number 206.

Importantly, at this stage, the hardware disclosed in the embodiment simply routes an instruction word in a particular position in register 130, to the pipeline execution unit according to what the "pipeline number" specifies (pipeline identifier within the template field). The "software" association between the instruction and the pipeline identifier are primarily determined at compile time. P. 6, lines 14, p. 6, lines 12-21. Because the hardware routing depends primarily on the pipeline identifier (within the template field), it can be said, that during execution, what ever instruction word is residing at position W6, for example, will be routed to pipeline execution unit 201. That is, the pipeline identifier is associated with the specific position in the register.

For example, suppose the compiler specifies pipeline identifier 1 (ALU) for instruction word W6, and places an ALU instruction in instruction word W6. During execution, the ALU instruction (W6) is routed to pipeline execution unit 201 (ALU). However, if the compiler specifies pipeline identifier 1 (ALU), but for some reason instruction word W6 were actually a Floating Point (FP) instruction, not an ALU instruction, the FP instruction W6 would still be routed to the ALU. This demonstrates that the pipeline identifier

(within the template field) determines the mapping of a position within register 130 to an execution unit type. This will be illustrated via the example below.

Accordingly, because the specification discloses mapping of positions within a register to execution units, the rejection under 35 USC §112, ¶1 is traversed.

II. The Hull Patent

It is asserted that what the Hull patent discloses is irrelevant to the present 35 USC 112, ¶1 issue. Specifically, the determination of the meaning of a term in a claim should only be determined by the specification of the instant invention. As disclosed above, from a hardware point of view, the pipeline identifier (within a template field) specifies that whatever instruction is located a particular location or slot within the register, that instruction will be routed to a pipeline execution unit of a given type.

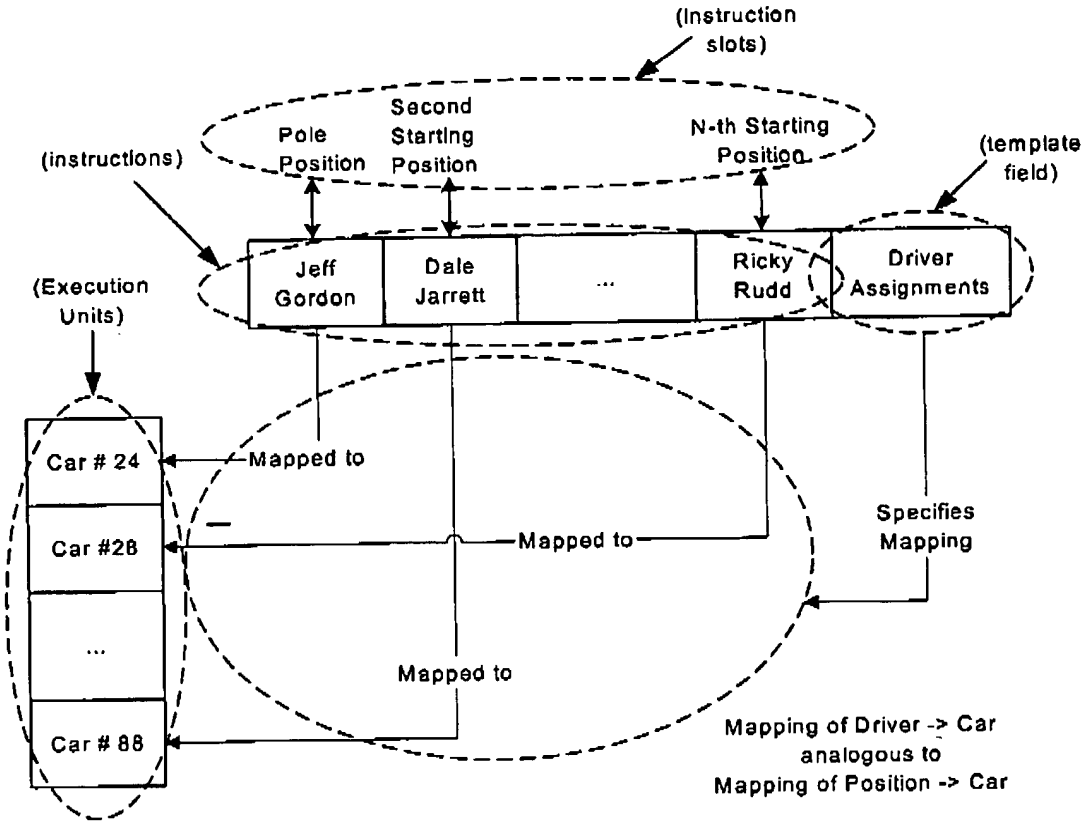
Even if Hull could be considered relevant to the 112 issue here, Hull performs similarly, if not identically, to the embodiment of the present invention. The Examiner's question appears to be whether an instruction OR an instruction slot is mapped to an execution unit type. The answer is BOTH, as will be illustrated via the example below.

Hull specifies that a compiler is used to determine the instructions in a bundle, their location within the bundle, and the template fields. Col. 5, lines 9-30. The template fields are an encoding of mapping of instruction slots within a bundle 30 to execution unit types. Col. 3, lines 63-66. Accordingly, from a hardware point of view, whatever instruction is stored in a particular slot within the bundle, that instruction will be routed to a specified pipeline execution unit type. This is the same as the instant invention, accordingly, the rejection under 35 USC §112, ¶1 is traversed.

III. Daytona 500 Example

As an analogy, consider the Daytona 500 race. For NASCAR races, Jeff Gordon drives Car #24 and Dale Jarrett drives Car #88. Further, there are time trials to determine the pole position (first starting position) and the starting line-up in the race. Suppose Jeff Gordon comes in with the fastest time and Dale Jarrett comes in with the second fastest time during time trials. In this case, Gordon would get the pole position and Jarrett would get the second starting position.

The analogy is as follows: Jeff Gordon (an instruction) is assigned to drive (via a template field) Car #24 (an appropriate execution unit); and Dale Jarrett (another instruction) is assigned to drive (via the template field) Car #88 (an appropriate execution unit). After the time trials (compiling) it is determined that that Jeff Gordon (an instruction) sits at the pole position (instruction slot 0); and Dale Jarrett (another instruction) sits at the second starting position (instruction slot 1). The diagram below illustrates the analogy:



Applying this analogy to the present invention embodiment, after compiling (the time trials) a first instruction (Jeff Gordon) is placed in a first instruction position (the pole position), and the first instruction (Jeff Gordon) is mapped via the template field to an appropriate execution unit (Car #24). Further, a second instruction (Dale Jarrett) is placed in a second instruction position (the second starting position), and the second instruction (Dale Jarrett) is mapped via the template field to an appropriate execution unit (Car #88).

Hull does the same thing. After compiling (the time trials) a first instruction (Jeff Gordon) is placed in the first instruction slot (the pole position), and the pole position (Jeff Gordon) is mapped via the template field to an appropriate execution unit (Car #24). Further, a second instruction (Dale Jarrett) is placed in the second instruction slot (the second starting position), and the second starting position (Dale Jarrett) is mapped via the template field to an appropriate execution unit (Car #88).

Thus, as seen in the analogy above, whether one uses the reference term "Jeff Gordon" or the "pole position," Jeff Gordon will still be mapped to Car #24. Also whether one uses the reference term "the second starting position" or "Dale Jarrett," Dale Jarrett will still be mapped to Car #88. In the same way, in the present embodiment, regardless of whether one uses the reference term "instruction word W0" (Jeff Gordon) or "instruction slot 0" (pole position), instruction W0 will still be mapped to the specified execution unit (Car #24).

Accordingly, because referring to a specific instruction that is stored in a particular instruction slot is synonymous to referring to the5 particular instruction slot, the specification discloses mapping of positions within a register to execution units. The rejection under 35 USC §112, ¶1 is therefore traversed.

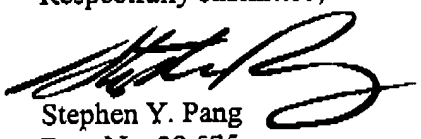
CONCLUSION

In view of the above, applicant believes that the rejections and objections have fully been traversed and that the pending claims are in condition for allowance.

Applicants also respectfully renew their request to the Examiner that he declare an interference with the '065 patent. Applicants also respectfully request that the examination of the present application be conducted with special dispatch, per 37 C.F.R. §1.607(b).

If the Examiner has any questions whatsoever, please contact the undersigned at the phone number listed below.

Respectfully submitted,



Stephen Y. Pang
Reg. No. 38,575

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300

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